UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/001,749	10/31/2001	Anirban Chatterjee	AUS920010915US1	4336

7590 06/15/2004	EXAMINER
Duke W. Yee	BONZO, BRYCE P

ART UNIT	PAPER NUMBER
2114	3

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DATE MAILED: 06/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/001,749	CHATTERJEE ET AL.
	Examiner	Art Unit	
	Bryce P Bonzo	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on <u>31 October 2001</u>.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) <u>1-21</u> is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) <u>1-21</u> is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on <u>29 January 2002</u> is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

NON-FINAL OFFICIAL ACTION

Status of the Claims

Claims 1-21 are rejected under 35 USC §103.

Rejections under 35 USC §103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamashita (United States Patent Application Publication No. 2002/0010882) in view of Vachon (United States Patent No. 6,681,348).

As per claims 1, Yamashita discloses:

A method of executing a hardware dump, comprising:

identifying a set of hardware dump information elements to collect (column 2, lines 44-53);

building the dump list in the allocated memory (column 6, lines 51-67).

Yamashita does not explicitly disclose: calculating an amount of memory to allocate for a dump list based on the identified set of hardware dump information elements. Vachon discloses these elements at Page 2, ¶24-25. Yamashita is concerned with transmitting as little data as possible remotely so as to speed up the transfer of diagnostic data. Vachon makes use of block allocation for data sizes to facilitate the high speed buffering of data in a transmission system carrying diagnostic data away from a processor core and scan chain. Thus it would have been obvious to one of ordinary skill in the art at the time of invention to incorporate the memory allocation features of Vachon into the mini-dump system of Yamashita and in doing so create an even faster core diagnostic data transfer system.

As per claims 2-10, Yamashita discloses:

2. The method of claim 1, further comprising: collecting the hardware dump information elements; and saving the collected hardware dump information elements in memory (column 4, lines 51-56).

3. The method of claim 1, wherein the step of identifying a set of hardware dump information elements comprises determining a dump mode (column 4, lines 51-56).

4. The method of claim 3, wherein the step of identifying a set of hardware dump information elements comprises identifying a complete set of static arrays if the dump mode is a complete dump (column 6, lines 57 through column 7, line 23).

5. The method of claim 3, wherein the step of identifying a set of hardware dump information elements comprises identifying a subset of static arrays if the dump mode is an abbreviated dump (column 7, lines 51 through column 8, line 2).

6. The method of claim 1, wherein the step of identifying a set of hardware dump information elements comprises identifying a set of static arrays (column 9, lines 10-23).

7. The method of claim 6, wherein the set of static arrays comprises a component static array for each component to be scanned (column 9, lines 24-40).

8. The method of claim 7, wherein each component static array comprises a set of constants, each constant representing a hardware dump information element to be collected (column 9, lines 24-40).

9. The method of claim 1, wherein the step of building the dump list comprises building the dump list based on the set of hardware dump information elements (column 9, lines 41-51).

10. The method of claim 1, wherein the hardware information elements comprises at least one of a scan ring, a trace array, cache contents, and cache directory contents (column 4, lines 20-67: physical memory includes a cache, cache directory and the scan paths, that is all "physical memory").

Claims 11-20 are the apparatus for executing the method of executing a hardware dump of claims 1-10 and are rejected accordingly.

Claim 21 is the computer program product for executing the method for executing a hardware dump of claim 1 and is rejected accordingly.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bryce P Bonzo whose telephone number is (703) 305-4834. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system.   Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Bryce P Bonzo
Examiner
Art Unit 2114

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